	L #	Hits	Search Text	DBs	Time Stamp
1	L1	18	(("5773876") or ("5835988") or ("5862248") or ("5914529") or ("5994169") or ("6090644") or ("6165818") or ("6307258") or ("20020027268")).PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/11 15:04
2	L2	2	("6787388").PN.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/11 16:07
3	L3	878	lead adj frame and (encapsulant or encapsulating) and heat adj sink	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/11 16:07

	L #	Hits	Search Text	DBs	Time Stamp
4	L4	258	3 and ((fold or folding or folded or bend or bending or bent) near4 (leadframe or "lead frame" or leads or pins))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/11 16:58
5	L5	217	4 and ((@ad<"20000907") or (@rlad<"20000907"))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/11 16:59
6	L6	4	5 and ESD	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/11 17:02

	L #	Hits	Search Text	DBs	Time Stamp
7	L7	4	4 and ESD	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/11 17:03
8	L8	217	5 and (encapsulating or encapsulated or encapsulant)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	2005/05/11 17:03

US-PAT-NO: 6213747

DOCUMENT-IDENTIFIER: US 6213747 B1
See image for Certificate of Correction

TITLE: Package stack via bottom leaded plastic (BLP) packaging

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Abstract Text - ABTX (1):
A packaged semiconductor device has bottom surface leads having portions of the package adjacent the lead edges excised. The outer leads may take the form of inverted-J leads, short stub **leads, vertically bent leads**-in-grooves, or may be entirely eliminated. Lead connections are on the bottom package surface, over the top package surface, and/or on the sides and ends of the package, enabling vertical stacking of the devices and simultaneous/alternative coplanar horizontal connections to other semiconductor devices, circuit boards, etc. A mold assembly with a castellated inner surface forms a package with alternating grooves and columns for holding side and end electrical connection surfaces.

Application Filing Date - AD (1):
19990621

Brief Summary Text - BSTX (10):
This type of construction has several disadvantages. First, the outer leads 24B of the superposed device 10B must be **bent differently from outer leads** 24A of the underlying device 10A. Thus, the devices 10A and 10B cannot be interchanged, and the outer leads 24B of device 10B are not configured for attachment to a PCB.

Brief Summary Text - BSTX (18):
The external package configuration may be used with any internal configuration of dice, leads, insulative layers, **heat sinks,** die-to-lead

connections, etc. Thus, the internal assembly configuration may comprise a Leads-Over-Chip (LOC), Chip-Over-Leads (COL), single or multiple die, wire bonded leads and/or tape-automated bonding (TAB) as well as other variations or combinations in construction.

Brief Summary Text - BSTX (20):

The outer lead is then an outward extension of the intermediate portion. The intermediate portion provides a bonding surface for joining to a circuit board, device, etc. In a further improvement of the invention, the **encapsulant** adjacent the edges of the intermediate lead portion is excised to a depth equaling about 0.1-1.0 of the lead thickness. The excised portion may take a variety of configurations.

Brief Summary Text - BSTX (22):

In another improvement, a semiconductor package is formed with castellated sides and/or ends whereby the outer **leads are bent** upwardly to fit in the castellation grooves, while extending slightly from the grooves to provide bonding sites for electrical connection to other devices, etc. A mold assembly is described, infra, for producing the castellated package.

Drawing Description Text - DRTX (17):

FIG. 16 is a partial end view of a transfer mold assembly for **encapsulating** a semiconductor device of the invention;

Drawing Description Text - DRTX (18):

FIG. 17 is a partial end view of a transfer mold assembly of the invention for **encapsulating** a semiconductor device with a castellated package for enclosing outer leads; and

Detailed Description Text - DETX (3):

With reference to the drawings of FIGS. 5-18 which describe the instant invention, and particularly to FIGS. 5 and 6, a pair of semiconductor devices 100 are shown in cross-section. In each device 100, the particular

configuration of die 102, metallized **lead frame** 104, and die-to-lead attach method may be any of the wide variety of known constructions in the art. As represented in FIGS. 5 and 6, a chip-over-leads (COL) interior construction with inverted-J (IJ) outer leads 118 is shown with inner leads 106 conductively connected to die pads 108 by wires 110. An intermediate lead portion 112 is positioned during encapsulation, e.g. transfer molding, to have a bottom lead surface 114 generally coplanar with the bottom package surface 116 of the molded polymer package 120. The bottom lead surface 114 of the intermediate lead portion 112 of each lead comprises a bonding surface for conductive connection to a semiconductor device, a circuit board, or other conduit or electrical apparatus. Each lead is separated from adjacent leads by a spacing 122 which may vary along the length of the lead. Preferably, the spacing 122 of the outer leads 118 is uniform.

Detailed Description Text - DETX (19):

Turning now to drawing FIGS. 12 and 13, a small-footprint semiconductor device 100 is shown with intermediate lead portions 112 having bottom lead surfaces 114 generally coplanar with the polymeric bottom surface 116 of the molded package 120. The package 120 has a vertical groove 156 aligned with each outer lead 118 such that the outer **lead may be bent** upwardly to fit within the groove. Between each groove 156 is a column 157 of the package 120. Thus, the semiconductor device 100 will be no larger, or just barely larger, than the molded package 120.

Detailed Description Text - DETX (20):

As shown in drawing FIGS. 12 and 13, outer leads 118A from the transfer molding process extend outwardly from the molded package 120. Vertical grooves 156 are premolded or formed after removal from a mold. Each outer **lead 118A is**

bent upwardly at bend 118B. The outer end 118C is closely fitted within the groove 156 near the top surface 117 of the molded package 120, and a portion 118D of the **lead in the area of bend** 118B typically extends a short distance outwardly from the groove to provide a bonding surface for lateral electrical connection to another semiconductor device, electrical conduit, or electrical apparatus. Each groove 156 is shown as extending to the top surface 117 of the package 120, with a groove depth 152 generally about equal to the lead thickness 132, and a groove width 154 slightly larger than the lead width 133, whereby the outer lead 118 will readily fit into the groove 156. Thus, the semiconductor device 100 has "surface" leads both on its bottom surface 116 and on surfaces of the sides 119 and/or ends 142.

Detailed Description Text - DETX (26):
Drawing FIG. 16 shows a mold assembly 160 for **encapsulating** the die/**lead frame** assembly 162 in polymer to form the semiconductor package 120. The die/leadframe assembly 162 is shown as including a die 102, leadframe 104, bond wires 110, and insulative tape 158.

Detailed Description Text - DETX (28):
Mold cavity 164 is defined by an inner surface 166A of the top plate 160A and an inner surface 166B of the bottom plate 160B. A polymeric **encapsulant** is introduced as a hardenable fluid through openings (not shown) as known in the art.

Detailed Description Text - DETX (31):
However, the particular groove/column pattern may also be produced in the molding step, using a mold assembly 170 as illustrated in drawing FIGS. 17 and 18. A wall 168 of the top plate 170A which is intersected by intermediate lead portions 112 has a pattern of alternating mold grooves 176 and mold columns 178. During the molding process, the mold grooves 176 are filled

with
encapsulant and become the package columns 157. Likewise, the spaces occupied
by the mold columns 178 become the package grooves 156 into which the outer
leads 118 are bent upwardly.

Detailed Description Text - DETX (32):
While drawing FIG. 12 depicts the package grooves 156 with square corners,
the preferred mold grooves 176 have angled groove sides 180 for easy release of
the hardened package from the mold cavity 172. The groove angle 182 may be any
angle which permits rapid package release, but will generally be in the range
of 5-15 degrees, depending upon the surface roughness of the mold cavity 172
and the particular **encapsulant** being used.

Detailed Description Text - DETX (35):
b. preparing a die-leadframe assembly including electrical connections
between the die and leadframe, any insulative layers, **heat sink,** etc.;

Detailed Description Text - DETX (37):
d. closing the mold assembly and injecting fluid polymeric **encapsulant** to
fill the mold cavity;

Detailed Description Text - DETX (38):
e. curing the **encapsulant** and removing the package from the mold;

Detailed Description Text - DETX (41):
h. **bending (if necessary) the outer leads** to the specified configuration.

Claims Text - CLTX (1):
1. A mold assembly for **encapsulating** a die and leadframe of a semiconductor
device in a polymeric package by transfer molding, comprising:

Claims Text - CLTX (3):
a generally planar, pressure-resisting bottom mold plate configured to be
sealably joined to said top mold plate, said top mold plate and said bottom
mold plate together forming a mold cavity with a top, a bottom, side walls and

end walls, said top and bottom mold plates configured to suspend a die and
leadframe by said leadframe within said mold cavity for injection of **encapsulant** thereinto,

Related Application Filing Date - RLFD (1):
19970709